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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/626,574	07/27/2000	Michael R. May	SIG000049	9605

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EXAMINER
LUU, AN T

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/626,574	MAY, MICHAEL R.	
	Examiner	Art Unit	
	An T. Luu	2816	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6,9,13-15 and 17* is/are rejected.

7)☒ Claim(s) *2-3,7-8,10-12,16 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Applicant's Appeal Brief filed on 4-7-03 has been received and entered in the case. The rejections set forth in the previous Office Action are maintained. The same ground of rejections is presented. Basic to reject claim 17 is rewritten to overcome a typographical error in the previous Office Action. Rejection of claims 5 and 14 under 35 USC 112 is introduced to establish Examiner's position of claim interpretation.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 5 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 appears to be incomplete because there is no structurally and/or operationally relationships of "an inverter" to the rest of the circuit. And "a controlled impedance" seems to be referred to "a gating circuit". Based on figure 2 of the instant application. Examiner considers an input of "an inverter" being coupled to "a gating circuit" and "a controlled impedance" is a component of "a gating circuit". Claim 14 has the same problem as that of claim 5.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 6, 9 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by the Farrell et al. reference (U.S. Patent 5,510,740).

The Farrell et al discloses in figure 8 an apparatus comprising a filter module 820 operatively coupled to received an input logic signal (output of 816 via a reset signal at 802) for producing a pulse signal 826; and a latch module 824 operative coupled to receive the pulse signal for latching the pulse signal as claimed in claims 1 and 6.

As to claim 9, element 816 is seen as a processing module and an input gating device is inherent with respect to reset signal since figure 9 and associated description on col. 22, lines 10-24 disclose the reset signal is ON/ OFF in periods lasting for more than several cycle of clock signal.

As to claim 15, Okada discloses signal at line 802 is a reset signal as required claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4, 5, 13-14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Farrell et al. reference (U.S. Patent 5,510,740) in view of the Okada reference (U.S. Patent 4,306,198).

The Farrell et al discloses all the claimed invention except for having a filter element comprising specific components being configured as required in claim 4. Okada discloses in figure 3 an apparatus comprising a capacitor C coupled to the input T1 and a gating circuit (Q5 and Q6), for generating the pulse signal (collector terminal of Q6), wherein the collector and an impedance of at least Q5, Q6 are tuned based on the rise time and fall time of the input signal (C, Q5 and Q6 is configured as identical as configuration of 46, 36 and 38 of figure 2 of the instant application) as required by claim 4. It would have been obvious to one skilled in the art to replace a generic filter circuit disclosed by Farrell by the one taught by Okada because the skilled artisan in the art would easily recognize that a filter circuit can be implemented in many different ways in the art without patentable distinction. The selection among different designs of a filter is seen as a design expedient dependent upon the particular requirement of the application.

As to claim 5, Okada discloses a drive transistor Q1 coupled "a controlled impedance" Q6 of the gating circuit. Okada does not disclose an inverter coupled between the gating circuit and the drive circuit as required by claim 5. However, it is well known in the art that inverter merely for reshaping a logic (i.e., inverting) of a signal. Thus, it would have been obvious to one skilled in the art to insert an inverter at gate of the driver transistor for providing a complementary signal at the output of the drive transistor. Inserting an inverter as such is seen as matter of routine electronic design as to accommodate a different type of transistor (i.e., n-type vs. p-type or vice versa).

As to claim 13-14, the scopes of these claims are similar to that of claims 4 and 5, respectively. Therefore, they are rejected for the same reasons set forth above.

As to claim 17, the scope of this claim is similar to the combination scopes of claims 1 and 4-5. Thus, it is rejected for the same reasons set forth above.

Response to Arguments

7. Applicant's arguments filed 4-7-03 have been fully considered but they are not persuasive.

Regarding rejection of claims 1, 6, 9 and 15 under 35 USC 102(b), Applicant argued that the prior art (Farrell) does not teach or suggest the limitation "the filter module produces a **pulse** signal in response to an **edge** of the input logic signal" and Farrell teaches away from claim 1 because "the output of reset filter 820 is only applied to the reset leading edge detector 808 when the reset signal of reset signal of reset input line 802 is of a predetermined time duration because of the action of reset filter 820". And Applicant has concluded that "Farrell does not teach or suggest a filter module that produces a pulse signal in response to an edge of an input logic signal, as claimed by Applicant". Examiner respectfully disagrees with Applicant because figure 9 and associated description (col. 22, lines 20-24) disclose a pulse as shown on diagram line 920 and this pulse does not respond instantly at the rising edge of the reset signal. Rather, it is responded to the rising edge of the reset signal *after a predetermined time* (i.e., period 916). Therefore, Examiner believes that limitation "the filter module produces a **pulse** signal in response to an **edge** of the input logic signal" is anticipated by Farrell.

With respect to Applicant's position that Farrell's invention requires a clock signal to operate wherein Applicant's invention does not required one. Examiner does not dispute with the

above assertion. However, art rejection of claim (i.e., 35 USC 102 or 103) is based on the recitation of claims, not what is disclosed in the specification.

Regarding rejection of claims 2, 3, 7 and 12 under 35 USC 103(a) by Farrell in view of Tsukikawa. Argument for these claims are moot since claims 2, 3 and 12 deem to be allowable as of this Office Action.

Regarding rejection of claims 4, 5, 13, 14 and 17 under 35 USC 103(a) by Farrell in view of Okada. Applicant has argued that the independent claims (1 and 9) do not read on Farrell and it is not obvious to combine references to reject his dependent claims. Examiner's response noted above is applicable here.

Allowable Subject Matter

8. Claims 2, 3, 7, 8, 10-12, 16 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose an apparatus comprising elements being configured as recited in claims. Specifically, none of the prior art teaches or suggests, among other things, the following limitations:

- An input of the first inverting logic element is coupled to the output impedance, and the pulse signal is received at the coupling of the input of the first inverting logic element and the output impedance recited on claims 2, 12 and 18.
- A second filter module limitation as recited on claims 7, 10 and 16.

- The input gating device provides one of a plurality of input logic signals as the input logic signal as required by claim 11.
- Claim 3 and 8 are dependent claims of claims 2 and 7.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 703-308-4922. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

An T. Luu
5-3-03

TIMOTHY P. CALLAHAN
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